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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,294	06/27/2001	Rajeev K. Nalawadi	42390P11478	7596

8791 7590 01/26/2005

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EXAMINER	
WANG, ALBERT C	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 09/894,294	**Applicant(s)** NALAWADI ET AL.	
	Examiner Albert Wang	**Art Unit** 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)□ This action is **FINAL**. 2b)☒ This action is non-final.

3)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)□ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)□ Claim(s) _____ is/are objected to.

8)□ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)□ The specification is objected to by the Examiner.

10)□ The drawing(s) filed on _____ is/are: a)□ accepted or b)□ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)□ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)□ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)□ All b)□ Some * c)□ None of:

1.□ Certified copies of the priority documents have been received.

2.□ Certified copies of the priority documents have been received in Application No. _____.

3.□ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) □ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) □ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) □ Notice of Informal Patent Application (PTO-152)

6) □ Other: _____.

DETAILED ACTION

1. This Office action is in response to the amendment filed November 1, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray et al., U.S. Patent No. 5,802,318 ("Murray"), in view of Intel Corporation, "Universal Host Controller Interface (UHCI) Design Guide", Revision 1.1, March 1996 ("UHCI").

As per claim 1, Murray teaches a system comprising:

a processor coupled to a bus (fig. 1, processor 100 coupled to bus 110; col. 4, lines 21-29);

a memory coupled to the bus (fig. 1, memory 108);

an external bus controller coupled to the bus (fig. 1, serial bus host controller 130); and

a basic input-output system (BIOS) coupled to the bus (fig. 1, ROM 118; col.4, lines 32-39), the BIOS comprising an external bus support component causing polling of external bus enabled devices and to provide support for external bus enabled devices responsive to the polling (figs. 1 & 2, device such as keyboard 140; col. 10, lines 6-13).

However, Murray does not expressly teach that polling involves generating a periodic interrupt. UHCI teaches that BIOS sets up an external bus controller's scheduler (sec. 5.1, "Software that is run early in the boot process must be modified to … set up the USB controller's scheduler. This code is typically the system BIOS."), the execution of which causes interrupts to be generated (sec. 4, Interrupts). UHCI teaches further that USB defines the interrupt transfer type to support devices that "require a predictable service interval" such as keyboards and that each frame is allocated "enough time to complete all scheduled ... interrupt transfers" (sec. 1.1). In other words, devices such as USB keyboards are polled, or interrupt driven, at a periodic interval. Thus, at the time of the invention, it would have been obvious to one of ordinary skill in the art that Murray's polling of external bus enabled devices is achieved using UHCI's interrupt transfer which causes in the generation of periodic interrupts. A motivation for doing so would have been to use a USB defined data transfer type.

As per claim 2, Murray teaches the external bus support component is to provide support for external bus enabled devices until an operating system providing external bus support is loaded (col. 10, lines 6-13).

As per claim 3, Murray teaches the external bus enabled devices comprise at least one of a keyboard, a mouse, a floppy drive, a biometric device, a hard disk drive, a compact disk read-only memory (CD-ROM) player (fig. 1, keyboard 140 or mouse 142).

As per claim 4, Murray teaches the external bus controller is a Universal Serial Bus (USB) host controller (figs. 2, 3A&B, host controller 130 comprises USB logic); the external bus support component is a USB support component (col. 10, lines 6-13, BIOS supports host controller 130); and the external bus enabled devices are USB devices (fig. 2, devices have USB interfaces).

As per claim 6, Murray teaches the processor conforms to the 32 bit Intel Architecture (IA-32) and the periodic interrupt is a system management interrupt (SMI) (col. 4, lines 11-15; col. 10, lines 14-21).

As per claim 7, Murray teaches the processor is compatible with the 32 bit Intel Architecture (IA-32) (col. 4, lines 11-15).

3. Claims 8-12, 14-17, 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray et al., U.S. Patent No. 5,802,318 ("Murray"), in view of Intel Corporation, "Universal Host Controller Interface (UHCI) Design Guide", Revision 1.1, March 1996 ("UHCI"), and Chaiken, U.S. Patent No. 6,128,732.

As per claim 8, Murray teaches a system comprising:

a processor coupled to a bus (fig. 1, processor 100 coupled to bus 110; col. 4, lines 21-29);

a memory coupled to the bus (fig. 1, memory 108);

an external bus controller coupled to the bus (fig. 1, serial bus host controller 130);

an external bus enabled device coupled to the external bus controller (figs. 1 & 2, keyboard 140);

a basic input-output system (BIOS) coupled to the bus (fig. 1, ROM 118; col.4, lines 32-39), the BIOS having instructions which when executed cause the processor to perform operations comprising:

causing polling of the external bus enabled device (col. 10, lines 6-13); and

handling input produced by the external bus enabled device (col. 10, lines 14-21).

However, Murray does not expressly teach that polling involves periodically generating an interrupt. UHCI teaches that BIOS sets up an external bus controller's scheduler (sec. 5.1, "Software that is run early in the boot process must be modified to … set up the USB controller's scheduler. This code is typically the system BIOS."), the execution of which causes interrupts to be generated (sec. 4, Interrupts). UHCI teaches further that USB defines the interrupt transfer type to support devices that "require a predictable service interval" such as keyboards and that each frame is allocated "enough time to complete all scheduled ... interrupt transfers" (sec. 1.1). In other words, devices such as USB keyboards are polled, or interrupt driven, at a periodic interval. Thus, at the time of the invention, it would have been obvious to one of ordinary skill in the art that Murray's polling of external bus enabled devices is achieved using UHCI's interrupt transfer which causes periodic generation of interrupts. A motivation for doing so would have been to use a USB defined data transfer type.

UHCI further teaches maintaining a plurality of external bus device data in the memory (fig. 4, frame list in system memory; sec. 1.2, schedule constructed in host memory; fig. 4, example schedule), and using a portion of the memory responsive to the interrupt (sec. 1, "to receive data from the USB device, the Host Controller receives the data and then transfers it to the system memory pointed to by the command").

However, UHCI does not expressly teach the BIOS having instructions which when executed by the processor, obtain the portion of the memory to be used. Chaiken teaches executing BIOS instructions to obtain a portion of memory to support USB (fig. 3A, steps 310, 312 & 318; fig. 3B, steps 322-324; col. 7, lines 22-33; fig. 4, memory is portioned). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Chaiken's obtaining a portion of memory to Murray/UHCI's system, as system memory provides faster access times (Chaiken, col. 1, lines 46-52)

As per claim 9, Murray teaches the processor conforms to the 32-bit Intel Architecture (IA-32) and the interrupt is a system management interrupt (SMI) (col. 4, lines 11-15; col. 10, lines 14-21).

As per claim 10, Murray teaches disabling an operation once software and drivers for external bus device support are loaded (col. 8, lines 45-58). Such software and drivers are loaded with the operating system (col. 7, lines 59 – col. 8, lines 4). Thus, it would have been obvious to disable the periodically generated interrupt when it is no longer needed.

As per claim 11, Chaiken teaches de-allocating a portion of memory when code in that portion is no longer needed, in order to leave space for software applications (col. 1, line 60 – col. 2, line 5). When an operating system providing external bus device support is completely loaded, it is obvious that the code in the portion of memory is redundant, and is no longer needed.

As per claim 12, Murray teaches the external bus controller is a Universal Serial Bus (USB) host controller (figs. 2, 3A&B, host controller 130 comprises USB logic); the external bus support component is a USB support component (col. 10, lines 6-13, BIOS supports host controller 130); and the external bus enabled devices are USB devices (fig. 2, devices have USB interfaces).

As per claim 14, Murray teaches a method comprising:

causing polling of one or more USB devices by an external bus support component (col. 10, lines 6-13; fig. 2, devices have USB interfaces); and handling input produced by one or more USB devices (col. 10, lines 14-21).

However, Murray does not expressly teach that polling involves periodically generating an interrupt. UHCI teaches that BIOS sets up an external bus controller's scheduler (sec. 5.1, "Software that is run early in the boot process must be modified to … set up the USB controller's scheduler. This code is typically the system BIOS."), the execution of which causes interrupts to be generated (sec. 4, Interrupts). UHCI teaches further that USB defines the interrupt transfer type to support devices that "require a predictable service interval" such as keyboards and that each frame is allocated "enough time to complete all scheduled ... interrupt transfers" (sec. 1.1). In other words, devices such as USB keyboards are polled, or interrupt driven, at a periodic interval. Thus, at the time of the invention, it would have been obvious to one of ordinary skill in the art that Murray's polling of external bus enabled devices is achieved using UHCI's interrupt transfer which causes periodic generation of interrupts. A motivation for doing so would have been to use a USB defined data transfer type.

UHCI further teaches maintaining a plurality of external bus device data in the memory (fig. 4, frame list in system memory; sec. 1.2, schedule constructed in host memory; fig. 4, example schedule), and using a portion of the memory responsive to the interrupt (sec. 1, "to receive data from the USB device, the Host Controller receives the data and then transfers it to the system memory pointed to by the command").

However, UHCI does not expressly teach BIOS having instructions which when executed by the processor, obtain the portion of the memory to be used. Chaiken teaches executing BIOS instructions to obtain a portion of memory to support USB (fig. 3A, steps 310, 312 & 318; fig. 3B, steps 322-324; col. 7, lines 22-33; fig. 4, memory is portioned). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Chaiken's obtaining a portion of memory to Murray/UHCI's system, as system memory provides faster access times (Chaiken, col. 1, lines 46-52)

As per claims 15-17, since Murray/UHCI/Chaiken teaches the system of claims 9-12, Murray/UHCI/Chaiken teaches the claimed method.

As per claim 19, UHCI teaches control transfers to one or more USB devices using the portion of the memory (sec. 1.1, Data transfer types; sec. 1.2, schedule constructed in host memory; fig. 4, example schedule)

As per claim 23, UHCI teaches adjusting the frame bandwidth of interrupt transfers based on data traffic involving the one or more USB devices (sec. 1.3, Scheduling). Consequently the rate of the interrupt is adjusted.

4. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray/UHCI/Chaiken as applied to claim 14 above, and further in view of Eichler, Jr. et al., U.S. Patent No. 6,772,252 ("Eichler").

As per claim 20, Chaiken teaches removing code from memory when the code is no longer necessary (col. 1, line 60 – col. 2, line 5), but does not expressly teach determining whether an operating system providing USB device support is loaded. Eichler teaches determining whether an operating system provides USB support (fig. 7, step 704). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Eichler's determining to Murray/UHCI/Chaiken's method. A motivation for doing so would have been to determine when code is no longer necessary.

As per claim 21, UHCI teaches checking a frame list base address register value to determine whether it is set to the address of the portion of the memory (fig. 3; secs. 1.2.1 & 1.4.1).

5. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murray/UHCI/Chaiken as applied to claim 14 above, and further in view of "Universal Serial Bus PC Legacy Compatibility Specification", Draft Revision 0.9, May 30, 1996 ("USBLegacy").

As per claim 22, Murray teaches disabling of emulation logic (col. 8, lines 45-58), but does not expressly teach this as disabling of USB legacy support. USBLegacy teaches the step of disabling when transitioning from legacy mode support to extrinsic mode (sec. 4.1.1-3; sec. 6.1.1). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the specification of USBLegacy to the Murray/UHCI/Chaiken's method, as the specification is well known in the art. UHCI teaches a register for disabling the hardware generated USB interrupts (sec. 2.1.3).

6. Claims 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray et al., U.S. Patent No. 5,802,318 ("Murray"), in view of Intel Corporation, "Universal Host Controller Interface (UHCI) Design Guide", Revision 1.1, March 1996 ("UHCI"), Chaiken, U.S. Patent No. 6,128,732, and Gharda et al., U.S. Patent No. 6,560,702 ("Gharda").

As per claim 24, Murray teaches a method comprising:

causing polling of an external bus enabled device by BIOS (col. 10, lines 6-13; fig. 2, devices have USB interfaces); and handling input produced by the external bus enabled device responsive to the polling (col. 10, lines 14-21).

However, Murray does not expressly teach that polling involves periodically generating an interrupt. UHCI teaches that BIOS sets up an external bus controller's scheduler (sec. 5.1, "Software that is run early in the boot process must be modified to … set up the USB controller's scheduler. This code is typically the system BIOS."), the execution of which causes interrupts to be generated (sec. 4, Interrupts). UHCI teaches further that USB defines the interrupt transfer type to support devices that "require a predictable service interval" such as keyboards and that each frame is allocated "enough time to complete all scheduled ... interrupt transfers" (sec. 1.1). In other words, devices such as USB keyboards are polled, or interrupt driven, at a periodic interval. Thus, at the time of the invention, it would have been obvious to one of ordinary skill in the art that Murray's polling of external bus enabled devices is achieved using UHCI's interrupt transfer which causes in the generation of periodic interrupts. A motivation for doing so would have been to use a USB defined data transfer type.

UHCI further teaches maintaining a plurality of external bus device data in the memory (fig. 4, frame list in system memory; sec. 1.2, schedule constructed in host memory; fig. 4, example schedule), and using a portion of the memory responsive to the interrupt (sec. 1, "to receive data from the USB device, the Host Controller receives the data and then transfers it to the system memory pointed to by the command").

However, UHCI does not expressly teach BIOS having instructions which when executed by the processor, obtain the portion of the memory to be used. Chaiken teaches executing BIOS instructions to obtain a portion of memory to support USB (fig. 3A, steps 310, 312 & 318; fig.

3B, steps 322-324; col. 7, lines 22-33; fig. 4, memory is portioned). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Chaiken's obtaining a portion of memory to Murray/UHCI's system, as system memory provides faster access times (Chaiken, col. 1, lines 46-52)

Lastly, while Chaiken teaches a BIOS ROM which may be reprogrammed (fig. 1, flash ROM 78; col. 5, lines 50-55), Murray/UHCI/Chaiken does not expressly teach a machine readable medium having instructions for the updating of BIOS to support the method steps above. Gharda teaches a machine readable medium for "re-flashing" of flash ROM to provide an updated version of BIOS (col. 1, lines 53-65). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gharda's machine readable medium to Murray/UHCI/Chaiken's method, as "re-flashing" is common practice for updating BIOS code.

As per claim 25-28, since Murray/UHCI/Chaiken teaches the system of claims 9-12, Murray/UHCI/Chaiken/Gharda teaches the claimed machine readable medium.

7. Claims 5, 13, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray/UHCI as applied to claim 1 above, over Murray/UHCI/Chaiken as applied to claims 8 and 14 above, and over Murray/UHCI/Chaiken/Gharda as applied to claim 24 above, and further in view of Intel Corporation, "Instantly Available Power Managed Desktop PC Design Guide", Revision 1.2, September 25, 1998 ("IAPM").

As per claim 5, Murray/UHCI does not expressly teach memory mapping and BIOS implementation with regards to the ACPI specification. IAPM teaches a design guide for such implementation (Sec. 4, ACPI BIOS design considerations). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply IAPM's ACPI implementation to Murray/UHCI's system. A motivation for doing so would have been to facilitate power management (IAPM, Sec. 1.1).

As per claims 13, 18, and 29, IAPM teaches a non-volatile-sleeping (NVS) memory region (Sec. 4.2.2, ACPI Non-Volatile-Sleeping Memory).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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January 21, 2005

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